ABSTRACT OF THE DISCLOSURE

MECHANISM FOR ALLOWING PCI-PCI BRIDGES TO CACHE DATA WITHOUT ANY COHERENCY SIDE EFFECTS

A method, system, and apparatus for providing data to an I/O adapter from a PCI-to-PCI bus bridge is provided. In one embodiment, once the PCI-to-PCI bus bridge receives a request for data from the I/O adapter, the PCI-to-PCI bus bridge determines whether the requested data is contained within a cached memory within the PCI-to-PCI bus bridge. If the data is contained within the cached memory, then the requested data is provided to the I/O adapter from the cached memory. If the requested data is not within the cached memory, the data is fetched from system memory, then cached in the PCI-to-PCI bus bridge, and sent to the requesting I/O adapter. To ensure that the data in the cached memory within the PCI-to-PCI bridge is not stale, signals are received, periodically or aperiodically, by the PCI-to-PCI bridge from a PCI host bridge indicating whether the data contained within the buffers is stale. If the data is stale, then in some embodiments, the contents of all the buffers are cleared, while in other embodiments, only the contents of the buffers containing data that has been indicated to be stale is cleared.